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An Analytical Method for Fast Calculation of Inductor Operating Space for High-Frequency Core Loss Estimation in Two-level and Three-level PWM Converters

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***Abstract*— Along the advances of wide-bandgap power devices, the pulse width modulation (PWM) converters are developing towards higher switching frequencies in recent years. Accurate estimation of the high-frequency power losses of magnetic components, the core loss in particular, has been a challenge for PWM converters. While the conventional approaches based on Steinmetz Equation lose the accuracy in PWM excitations, the "loss map" approach has been proposed recently as a practical method to accurately estimate the inductor core loss. To calculate the core loss, the inputs of the loss map need to be retrieved from the steady-state inductor voltage/current waveforms. As a supplement to the loss map approach, this work proposes an analytical method to rapidly generate the inputs (inductor operating space) for the loss map to replace the efforts in building simulation models and experimental rigs. The proposed approach relies on the operation and modulation principles of PWM converters and enables computerized calculation of the operating space and the inductor core loss. The proposed approach is developed for both 2-level and 3-level converters and validated by experiments. The results reveal that a 3-level converter running the same inductor generates less than half the core loss compared to a 2-level converter, when the maximum current ripple is kept equivalent. The proposed approach is based on the operation principles of the converter topology and therefore can be applied generally regardless of the core material or the design of the inductor, as long as the loss map of the inductor is pre-produced.**

***Index Terms*—core loss, loss map, pulse width modulation, three-level converter, virtual prototyping**

I. Introduction

Inductors play an important role in power electronics, which have unneglectable contribution to both the volume/weight and the power loss of Pulse Width Modulation (PWM) converters [1]. As a result of the advances of Wide Bandgap power devices, the PWM converters are developing towards higher switching frequencies (e.g. >50 kHz) in recent years. Due to the high-frequency operation, the high-frequency power losses in the magnetic components, the core losses in particular, become significant. The prediction of the inductor core loss becomes increasingly important in achieving more accurate modeling in the optimization [2] and virtual prototyping [3] of power converters.

The power loss of an inductor consists of two parts: copper loss and core loss. While the high-frequency copper loss can be relatively accurately estimated by analytical models (e.g. [4]), the high-frequency core loss is more difficult to predict in PWM converters [5]–[9]. The particular challenges in the case of inductor core loss in PWM converters are caused by the PWM operations, which involves dc-bias (pre-magnetization) [7], varying pulse widths (duty cycles) [10] and rectangular excitation [11]. Due to the lack of fully-physical-based model, the estimation of core loss must rely on empirically measured data. The conventional approaches, e.g. Steinmetz Equation (SE), are based on only sinusoidal excitation without considering the dc-bias effect. Numerous efforts, including the improved Steinmetz Equations, have been made in the past decades to close the gap in the evaluation and prediction of the core loss in PWM converters [5]–[14].

To accurately predict the core loss for PWM converters, the state-of-the-art approach is to build up a "loss map" based on empirical B-H loop measurements with rectangular excitation [5], [8]. Loss map can be considered as a lookup table covering possible operating points of the inductor core exposed in rectangular excitation. The loss map approach is formed by two stages: (1) generate the loss map based on discrete measurements and interpolation (2) utilize the loss map to calculate core loss. Ideally, the loss map is established by the inductor manufacturer. On the users' side, the pre-built loss map acts as the datasheet for the calculation of the high-frequency inductor core loss in the design stage of a converter.

As a pre-step of utilizing the loss map, the steady-state PWM waveforms on the inductor need to be retrieved as the input for the loss map. In the existing studies, these waveforms are drawn from simulation models [5], [8], [14] for estimation purpose or experimental measurements [8], [9] for validation purposes. However, establishing and running the time-domain simulations are time- and resource-consuming. Besides, since the theoretical estimation is intended to reduce the cost of evaluation, constructing hardware to extract the waveforms is on the opposite of virtual prototyping [3]. This becomes more problematic in the case where many converter operating points/designs have to be evaluated, such as in an iterative optimization tool [2].

Hence, it is motivated to generate the inputs, i.e. the inductor operating spaces, analytically for the inductor core loss estimation. There are previous studies that presented analytical approaches of estimating the core loss, such as [15]–[18]. However, [15], [18] are based on Steinmetz Equation and

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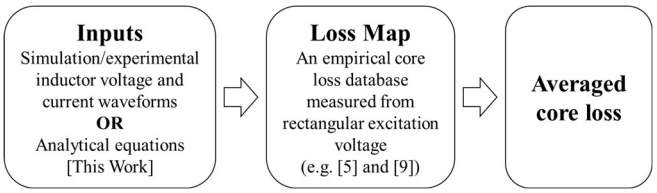


Fig. 1. Loss map calculation

improved Generalized Steinmetz Equation (iGSE), which have not considered the effect of pre-magnetization. In addition, these studies mainly focused on the line inductors in 2-level converter topology. In recent years, 3-level converters, such as the Neutral Point Clamped (NPC) [19], [20] and T-type converter (TNPC) converters [21], are drawing attentions both in academia and industry for low and medium voltage applications. Hence, this paper also intends to draw a comparison between the 2-level and 3-level converter from the inductor core loss point of view. The inductor operating spaces in these two topologies are also investigated.

The contributions of this paper are: (1) An analytical approach is proposed to generate the inputs (i.e. inductor operating space) to feed into a pre-built inductor loss map, in order to predict the inductor core loss under a certain operation point of the PWM converter. The analytical model generates the loss map inputs through iterative mathematical operations to replace the inductor PWM voltage/current waveforms conventionally captured from experiments and simulations. (2) The difference between a 2-level and a 3-level converter regarding the filter inductor core losses is revealed based on the topologies' operation principles. As a supplement of the loss map approach (e.g. [5], [9], [12]), this work focuses on generating the loss map inputs as shown in Fig. 1, which is studying the operation of the PWM converter topology and the converter-load circuit. In contrast, [9] focused on the measurement/production of the core loss map, which is studying the characteristic of an inductor/a core material. The proposed approach can achieve a fast calculation of the inductor core loss in both 2-level and 3-level converters, which is beneficial in the modelling/virtual prototyping of PWM converter systems. Additionally, the proposed approach can be easily integrated into the existing numerical optimization tools of power converters such as [2]. The preliminary results of this work has been presented in [22] as a conference paper. This article will be presented in the following sequence: (1) review and introduction of the loss map approach. (2) analytical core loss calculation for 2-level and 3-level converter. (3) case study based on simulation (4) experimental evaluation.

II. Estimate Core Loss in PWM Converters

A. Review on core loss calculation for rectangular excitation

The main challenge of predicting the core loss is that there is no physical-based model that can accurately include all dynamic and nonlinear effects [6], [23]. Therefore, the available approaches for core loss modelling all rely on experimentally measured data. The differences between these approaches are mainly in two aspects

1. How the original core loss data is measured and formed. For example, the core loss data can be measured from sinusoidal excitation or rectangular excitation.
2. How to utilize the finite empirical data to predict the core loss of any given waveform

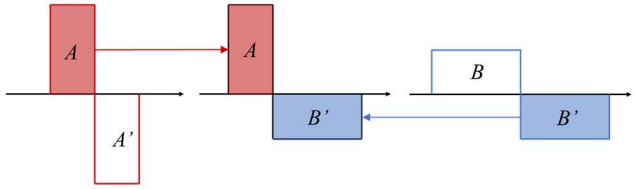


Fig. 2. Composite waveform hypothesis for core loss calculation

To calculate the core loss for rectangular excitation, the approaches reported in literature can be categorized as:

1. Apply Steinmetz Harmonic Analysis and look up the core loss data measured from sinusoidal excitation. This approach decomposes the rectangular excitation into harmonics through Fourier Analysis and adds up the core loss for each harmonic calculated through original Steinmetz Equation. This approach has been proven to lose accuracy in [24] due to the nonlinear nature of core loss.
2. Apply Improved Generalized Steinmetz Equation (iGSE) [6] or its variations and look up the core loss data measured from sinusoidal excitation. This type of approach utilizes the original Steinmetz-equation parameters measured from sinusoidal excitations to estimate the core loss of B-H loops decomposed from non-sinusoidal excitations. However, as stated by the author in [6], [13], iGSE is an approximation method relying on the original Steinmetz parameters, in which the accuracy is limited by the frequency-dependent best-fit SE parameters, especially in the case of waveforms containing harmonics crossing a wide range of frequency.
3. Apply Composite Waveform Hypothesis (CWH) or its variations and look up the core loss data measured directly from rectangular excitation. CWH is an important advance in modelling core loss in power electronics which was proposed in 2010.

CWH and rectangular-voltage-excited core loss data have been proven to have better accuracy and usability compared to the approaches based on SE and sinusoidal-excited core loss data as investigated in [11], [13], [24], [25]. Because CWH is important for this work's approach while it is still relatively less known, the concept of CWH is introduced as follows.

In one switching cycle of a power converter, the typical inductor voltage is illustrated as *S* in Fig. 2, which is an asymmetric rectangular waveform with different amplitudes and pulse widths in the positive and negative cycles. To calculate the core loss of waveform *S*, the CWH approach decomposes waveform *S* into standard segment *A* and *B'* where *A* is one positive segment and *B'* is one negative segment. The idea of CWH can be extended to decompose the whole PWM waveform over a fundamental cycle into positive and negative segments on switching cycle basis as applied in [8], [9].

Although CWH is verified to have excellent accuracy for an asymmetric waveform *S*, it was later pointed out in [11], [13], [24], [25] that CWH does not work well when there is OFF time

in the voltage waveform (zero voltage). However, in typical DC/AC PWM converters, the inductor voltage does not witness any zero voltage due to the varying fundamental-frequency component on the load side. Therefore, CWH can still be considered the most accurate approach to estimate the core loss in typical PWM converters.

With further investigations on this topic, it has been reported that the dc-bias can cause significant impact on the core loss [5]–[7], [26], while this effect is not included in iGSE [6] and the initial work on CWH [13]. With the dc bias effect included, the Loss Map approach has been proposed in [5], [8], [12] as the most recent advance on this topic, which shares the same principle as CWH in decomposing the PWM waveforms into segments and calculating core loss from data measured from rectangular excitation voltage. The loss map approach can be considered as the state-of-the-art for accurate estimation of core loss in PWM converters, which has the following merits:

1. Higher accuracy compared to SE based approaches because the core loss data are measured from rectangular excitation voltage
2. DC-bias effect can be included
3. Only symmetric voltage waveforms need to be measured (e.g. *AA'* and *BB'* in Fig. 2). This merit simplifies one dimension (duty ratio) of the core loss data measured from rectangular excitation voltage.
4. The calculation can be easily computerized and automated because it is performed on segment basis.

Although the core loss map generated from rectangular excitation voltage is currently unavailable from the manufacturers, it is the only option to achieve accurate core loss estimation that overcomes the drawbacks of Steinmetz-based approaches. Therefore, to achieve accurate core loss modelling, this work is based on the loss map approach.

B. Core loss measurement

The first part of the loss map approach is to establish a core loss database from discrete empirical measurements, which covers the operating points defined by three variables as

$$Q = f\left(\Delta B, \left|\frac{dB}{dt}\right|, H_0\right) \tag{1}$$

where $|dB/dt|$ is the flux density change rate; ΔB is the peak-to-peak amplitude of the flux density swing; H_0 the dc-biased magnetic field strength; Q is the core energy loss, e.g. in the unit of millijoules. The continuous loss map is produced from finite data points with interpolations.

To characterize the core loss, B-H loop measurement is widely used in previous studies [5], [7], [9], [27]. As the most important feature of this approach, only the core loss is measured out from the total inductor losses. To perform B-H loop measurement, an additional flux sensing winding is fitted on the inductor. The principle of this approach is to find the magnetic field H and flux density B on the inductor core by measuring the excitation current i_L and the open-circuit voltage on the sensing coil u_{L2} as

$$H(t) = N_1 \cdot i_L(t)/l_e \tag{2}$$

$$B(t) = \frac{1}{N_2 A_e}\int_0^t u_{L2}(t)\,dt \;\; (B(0) = 0) \tag{3}$$

where N_1 is the number of turns of the main winding of the inductor; N_2 is the number of turns of the flux-sensing winding; A_e is the effective cross-section area of the core; l_e is the effective length of magnetic path of the core. The core energy loss of a closed BH loop can then be found from (4) over the period of $2T$.

$$Q = A_e l_e \int H\,dB = \frac{N_1}{N_2}\int_0^{2T} i_L(t)\cdot u_{L2}(t)\,dt \tag{4}$$

A top-level illustration of the setup to perform B-H loop measurement is shown in Fig. 3. To drive the excitation current into the inductor-under-test, an excitation power converter is required. We have proposed a half-bridge based circuit to excite the inductor in [9]. This circuit allows a high excitation current to flow in both directions and enables the compensation of asymmetric inductor voltage caused by the voltage drops on power devices. The accuracy of B-H loop measurement is sensitive to the phase discrepancy between the current and voltage probes [5], [28]. In this work, the phase discrepancy between the voltage/current probes is aligned through a de-skew tool, Keysight U1880A.

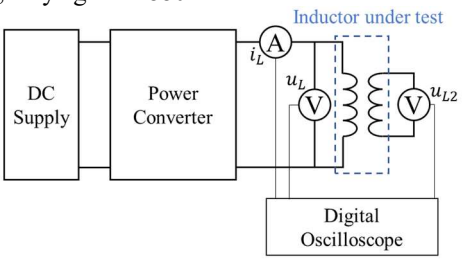


Fig. 3. B-H loop measurement

C. User-friendly loss map calculation

The second part of the loss map method is to calculate the core loss of a PWM waveform utilizing the empirical loss map. In [9], we have proposed the concept of a "user-friendly loss map" to improve the usability of loss maps. A user-friendly loss map is generated for one design of inductor (i.e. fixed core material, shape and winding arrangement) with the magnetic-domain variables in (3) converted to electrical-domain variables. The main benefit of the user-friendly loss map is to simplify the core calculation process by avoiding translating the inductor voltage current into magnetic domain, which requires accurate geometric information of the inductor, such as gap length, magnetic path length, cross section area and winding arrangement. The geometry information may not be available or cannot be accurately measured on the users' end, especially for the housed/potted inductors. For gapped cores, the user-friendly loss map also avoids the additional calculation associated with the existence of the air gap [29], and it includes the gap losses [9], [30] in the testing. Assuming a user-friendly loss map is available from the manufacturers, the users, e.g. power electronics engineers, only need to model the inductor voltage and current to achieve accurate core loss modelling.

As elaborated in [9], the user-friendly loss map calculation decomposes the PWM excitation into single-pulse segments as shown in Fig. 4. The segments are separated by the zero-crossings of inductor voltage $u_L(t)$ in Fig. 4, where a and b are the start and end point of one segment; U_L is the average main

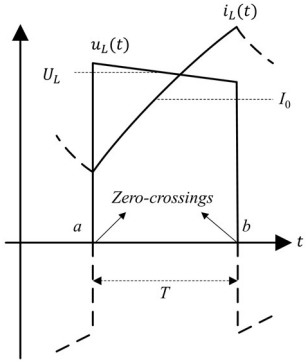


Fig. 4. A pulse segment for core loss calculation ($u_L(t) > 0$)

inductor winding voltage; I_0 is the dc-bias level of the inductor main winding current; T is the period of one pulse segment.

For one inductor design, both the magnetic core and the windings are fixed. The loss map of this inductor design can be reconstructed with electrical-domain input arguments, i.e. voltage and current values. The relationship between the two formats of loss map variables (conventional (1) vs. user-friendly) are shown in the following expressions

$$\Delta B = \frac{1}{N_2 A_e}\int_a^b u_{L2}(t)\,dt = \frac{U'_{L2}\cdot T}{N_1 A_e} \propto U'_{L2}\cdot T \quad (5)$$

$$\frac{\Delta B}{T} = \frac{1}{T}\frac{1}{N_2 A_e}\int_a^b u_{L2}(t)\,dt = U'_{L2}\cdot\frac{1}{N_1 A_e} \propto U'_{L2} \quad (6)$$

$$H_0 = \frac{1}{T}\cdot\frac{N_1}{l_e}\int_a^b i_L(t)dt = I_0\cdot\frac{N_1}{l_e} \propto I_0 \quad (7)$$

where $N1/N2$ is the turn ratio, u_{L2} is the secondary voltage on the sensing winding; U'_{L2} is the voltage scaled from the secondary side to the primary side with the turns ratio, which is averaged over the period of T, e.g. from a to b in Fig. 4. Note the voltage input for the user-friendly loss map could be either U_L or U'_{L2}, while U'_{L2} does not equal to U_L considering the winding voltage drop. In simplified simulations or analytical models in this work, only the main inductor voltage U_L is modelled for simplicity. To bypass the need of modelling the instantaneous winding voltage drop on the users' end, the core loss map can be constructed from the beginning with the main inductor voltage U_L as the index variable instead of U'_{L2}. To construct a loss map in this format, while the u_{L2} is measured to obtain the core loss through (3)-(4), the u_L is separately measured at the same time in the core loss testing illustrated in Fig. 3. In this way, one pulse segment described by a set of $|U_L|T$, $|U_L|$ and I_0 is linked to one core loss energy value measured from one dynamic BH loop. Subsequently, the loss map in (1) can be re-constructed into the user-friendly format for one inductor design as

$$Q = g(|U_L|T, |U_L|, I_0) \quad (8)$$

Note that the core loss for one pulse segment is assumed to be half of a corresponding closed dynamic BH loop produced from a symmetric full cycle of rectangular voltage [8], [9]. With the user-friendly loss map produced, the core loss of a given PWM waveform can be calculated. For each segment, the associated core loss can be found from the loss map by feeding the three inputs in (8) extracted from this segment. Then the calculation is repeated for each switching cycle and each single-pulse segments. Assuming the given PWM waveform is formed by N switching cycles and $2N$ pieces of pulse segments, the total core loss associated with the PWM waveform is obtained by adding up the core losses of all $2N$ segments as

$$Q_{total} = \sum_{n=1}^{2N} Q_{(n)} \quad (9)$$

In summary, to achieve the accurate and easy-to-use core loss estimation, the following concepts are applied in this work:

1. Apply CWH to decompose the PWM waveform
2. The core loss data is measured with rectangular excitation voltage, in which the voltage amplitude, the pulse width and the dc-bias current are considered
3. The core loss data is established on an inductor design in the form of a "user-friendly loss map"

Although the user-friendly core loss map is not available from manufacturers yet, it still enables the core loss estimation for arbitrary operating points of PWM converters out from finite core loss measurements performed in a stand-alone test rig. If the batch-to-batch variation [23] is neglected, the user-friendly loss map only needs to be measured on one sample that represents one inductor design, which is possible to be done by the manufacturers, especially for standardized inductors.

III. Analytical Core Loss Modelling

To estimate the core loss, the steady-state inductor voltage/current waveforms are required as the inputs for the loss map. As introduced, these waveforms can be drawn from simulation models for estimation purpose or experimental measurements for validation purpose. However, establishing and running the time-domain simulations are time- and resource-consuming. As the concept of virtual prototyping is advocated for designing power converters [3], the construction of hardware to extract the waveforms should be avoided. This becomes more problematic in the case where various converter operating points/designs have to be evaluated.

Alternatively, the core loss estimation can be conducted analytically and implemented in numerical computing tools. This work proposes an analytical method to calculate the core loss based on the pre-measured user-friendly loss map. The analytical model is developed for both a two-level converter and a three-level converter, of which the basic structures are shown in Fig. 5.

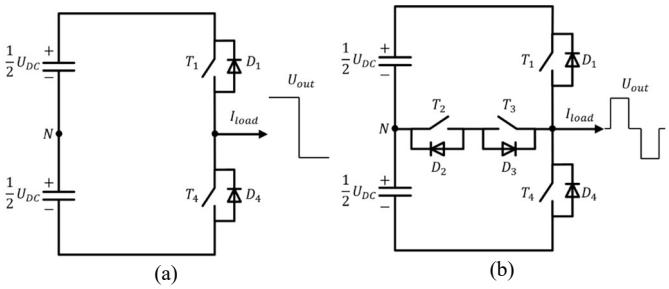


Fig. 5. Basic structure of (a) 2-level converter (b) 3-level T-type converter

A. Analytical model for a 2-level converter

Two representative single-phase two-level configurations are considered as the examples in this study. The first example is a

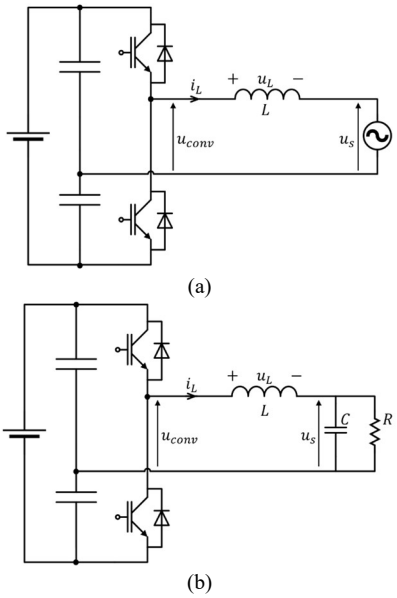


Fig. 6. Single-phase two-level inverters (a) Transformerless grid-tied PV inverter (b) Inverter with a passive load R and a low-pass LC filter

transformerless, single-phase, grid-tied photovoltaic (PV) inverter [20] as shown in Fig. 6(a), where the inductor is the grid interface line inductor. The second example is a single-phase inverter with a passive load R and a low-pass LC filter as shown in Fig. 6(b).

In both configurations, the operation of the inductor can be represented by the equivalent circuit shown in Fig. 7. The converter on one side is generating varying-duty-cycle square waves u_{conv} on switching cycle basis. The voltage on the other side can be treated as a sinusoidal voltage u_s with the fundamental frequency of f_0 for both systems, which is the grid voltage or the filtered load voltage. The parasitic resistance of the converter-load circuit is neglected for simplicity.

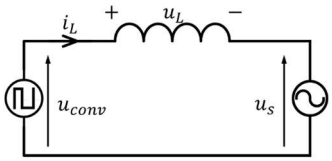


Fig. 7. Equivalent circuit for core loss calculation

In the equivalent circuit, the inductor voltage u_L is the difference between u_{conv} and u_s as

$$u_L(t) = u_{conv}(t) - u_s(t) \tag{10}$$

Assuming the converter carrier frequency $f_{SW} >> f_0$ (e.g. $f_{SW}/f_0 > 20$), the grid/load voltage u_s can be treated as constant in each switching cycle, which is annotated as U_s. Subsequently, the converter voltage and grid voltage in one switching cycle is considered as illustrated in Fig. 8(a). In the +DC cycle, the converter outputs $+U_{DC}/2$. In the −DC cycle, the converter outputs $-U_{DC}/2$. Applying the equivalent circuit in Fig. 7, the inductor voltage U_{L+}/U_{L-} in each switching cycle can be found by (11) and (12) for +DC/−DC cycles respectively, as illustrated in Fig. 8(b).

$$U_{L+} = \frac{U_{DC}}{2} - U_s \tag{11}$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \tag{12}$$

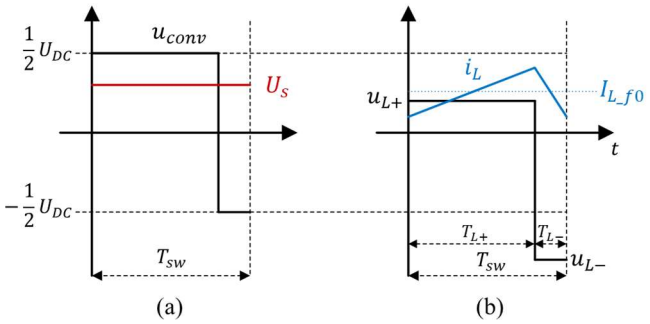


Fig. 8. Example of a 2-level converter in one switching cycle (U_{ref} >0) (a) converter output voltage u_{conv} and grid/load voltage Us (b) inductor voltage/current

In order to utilize the user-friendly loss map, the three inputs need be found for each segment, which are U_LT, U_L and I_0. As mentioned, the segments are separated by the zero crossings of the inductor voltage u_L. As shown in Fig. 8(b), the zero-crossing instants of u_L can be treated the same as the converter output voltage u_{conv}, assuming infinite rise/fall time. Therefore, in one switching cycle, the +DC cycle corresponds to the positive segment; the −DC cycle corresponds to the negative segment.

The time duration and duty cycles of u_{conv} can be found from the reference voltage of the converter, which is U_{conv_f0}. Assuming the conventional Sinusoidal Pulse Width Modulation (SPWM) applied, the duty cycles of the +DC/−DC cycles in one switching cycle can be calculated through (13) and (14).

$$D_{L+} = [\frac{U_{conv\_f0}}{(U_{DC}/2)} + 1]/2 \tag{13}$$

$$D_{L-} = 1 - D_{L+} \tag{14}$$

The time durations are found from the duty cycles by (15).

$$T_{L+/L-} = D_{L+/L-} \cdot \frac{1}{f_{sw}} \tag{15}$$

Thus, the U_LT and U_L can both be found from the modulation principle of the converter as explained. As for the DC-bias current I_0, it can be treated as the fundamental-frequency component of the inductor current I_{L_f0} as shown in Fig. 8(b).

Following the above process, the three inputs for the user-friendly loss map can be generated on switching cycle basis. As an example, assuming f_0 = 100 Hz and f_{sw} = 20 kHz, one fundamental cycle can be sliced up to N = 200 switching cycles. Each switching cycle contains one positive segment and one negative segment (unless T_{+DC} or T_{-DC} equals to zero when the peak reference voltage reaches the modulation boundaries). For the i_{th} (i = 1...N) switching cycle, three fundamental-frequency components are expressed as

$$U_s = U_{sm} \cdot \sin(\frac{i}{N} \cdot 2\pi) \tag{16}$$

$$I_{L\_f0} = I_{Lm\_f0} \cdot \sin(\frac{i}{N} \cdot 2\pi + \varphi_1) \tag{17}$$

$$U_{conv\_f0} = U_{convm\_f0} \cdot \sin(\frac{i}{N} \cdot 2\pi + \varphi_2) \tag{18}$$

where U_{sm}, I_{Lm_f0}, U_{convm_f0} are the amplitudes of the fundamental-frequency load/grid voltage, inductor current and converter output voltage; φ_1 and φ_2 are the phase angles referenced to the load/grid voltage. All these constants can be found from the operating model of the converter-load system. By inputting (11)-(18) into the loss map (8), the core loss of the

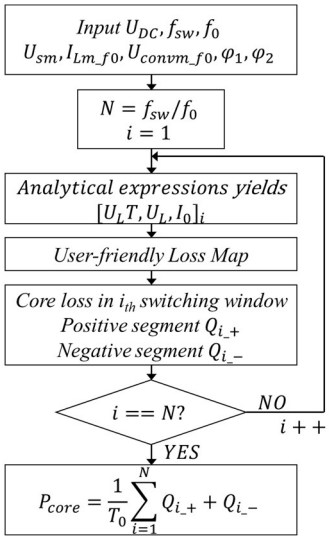


Fig. 9. Core loss computation process

i_{th} switching cycle can be calculated, which contains the core loss for the positive segment Q_{i_+} and the negative segment Q_{i_-} in the form of energy. In order to find the averaged core loss, the above process is repeated for each switching cycle over one fundamental cycle. Eventually, the core losses of all switching cycles are summed up to yield the total core loss of one fundamental cycle. The averaged core loss in power P_L can also be obtained. This whole process can be achieved by performing iterations in a numerical computing software, such as MATLAB, which is visualized in Fig. 9.

To summarize, for the analytical core loss estimation, the inputs of the loss map are found from the equivalent circuit shown in Fig. 7 at switching cycle level. To extract the inputs for the calculation, the amplitudes and phase angles of the fundamental-frequency components, i.e. U_{conv_f0}, I_{L_f0} and U_s, are found from the operating model of the converter-load system. The calculation is then repeated on switching-cycle-by-cycle basis to obtain the total core loss over a fundamental cycle.

The coefficients associated with the converter-load operation are the same as the required parameters in the analytical model of the power device losses, such as [2], [31], [32]. This feature enables the proposed core loss estimation to be directly integrated into a numerical modelling/optimization tool of a power converter, such as [2].

The proposed approach mainly models the rectangular converter output voltage and avoids modelling the instantaneous current ripple at switching period level. Current ripple prediction (e.g. [33], [34]) assumes that the inductance L is constant for simplification. The real-world inductor current shows a distorted "curvy" shape [5], [9] due to the non-linear core magnetization process, which cannot be modelled accurately. In contrast, the inductor voltage is relatively easier to be accurately modeled in a voltage source converter, especially in the case with fast-switching wide-bandgap devices where the converter output voltage is close to ideal rectangular voltage.

B. Analytical model for a 3-level converter

The above proposed analytical approach is extended to a 3-level converter. A 3-level converter outputs three voltage levels: positive DC rail U_{+DC}, neutral point voltage U_{NP} and negative DC rail U_{-DC}. With SPWM applied, in each switching cycle the ideal converter output voltage is formed by U_{+DC}/U_{NP} when $U_{ref} > 0$, or U_{-DC}/U_{NP} when $U_{ref} < 0$. Therefore, the inductor voltage is still a two-level square-wave within each switching cycle as shown in Fig. 10, which is a result of the converter output voltage shifted up/down due to the grid/load side voltage.

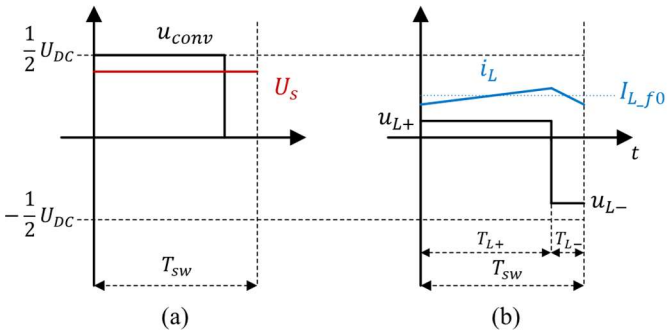


Fig. 10. Example of a 3-level converter in one switching cycle (U_{ref} >0)
(a) converter output voltage, grid/load voltage (b) inductor voltage/current

The duty cycles and inductor voltages can be found following the modulation principles of the 3-level converter. When $U_{conv\_f0} \geq 0$, the duty cycles are expressed as

$$D_{+DC} = U_{conv\_f0}/(U_{DC}/2) \tag{19}$$

$$D_{NP} = 1 - D_{+DC} \tag{20}$$

The amplitudes of the inductor voltages are calculated from the converter output voltage in this case and the grid voltage as

$$U_{L+} = \frac{U_{DC}}{2} - U_s \tag{21}$$

$$U_{L-} = 0 - U_s \tag{22}$$

When $U_{conv\_f0} \leq 0$, the duty cycles are found as

$$D_{-DC} = -U_{conv\_f0}/(U_{DC}/2) \tag{23}$$

$$D_{NP} = 1 - D_{-DC} \tag{24}$$

And the inductor voltages in this case are calculated as

$$U_{L+} = 0 - U_s \tag{25}$$

$$U_{L-} = -\frac{U_{DC}}{2} - U_s \tag{26}$$

Hence, by replacing equations (11)-(14) with (19)-(26) in the calculation flow in Fig. 9, the high-frequency core loss of the inductor in a 3-level converter can also be calculated on cycle-by-cycle basis.

C. Summary

The above developed analytical method enables the fast calculation of core loss for arbitrary operating point of a 2-level or 3-level PWM converter. Compared to capturing and

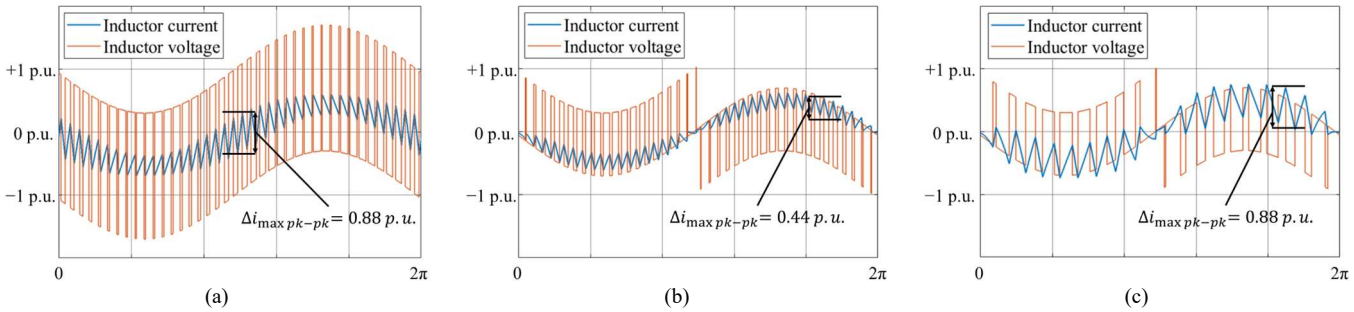


Fig. 12. Example of inductor voltage/current waveforms over a fundamental cycle with identical dc-link voltage, load and modulation index (a) 2-level converter with $f_{sw}/f_0 = 30$ (b) 3-level converter with $f_{sw}/f_0 = 30$ (c) 3-level converter with $f_{sw}/f_0 = 15$

analyzing the experimental/simulation waveforms, the proposed analytical calculation only requires the descriptive parameters of the converter-load system apart from the empirical core loss data, which are normally defined in the early design stage of a power converter system. The need of building real test rigs or simulation models are avoided in the proposed approach for the purpose of predicting the inductor core loss.

IV. Case Study by Simulation

A case study is conducted in this section based on ideal simulation modles to investigate the operation of the inductor depending on the converter configuration. The investigated inductor is a customized, high-current inductor with gapped EE cores built from Vacoflux 48 Cobalt Iron (CoFe) laminations as shown in Fig. 11. The loss map of this inductor was experimentally established in a previous study [9].

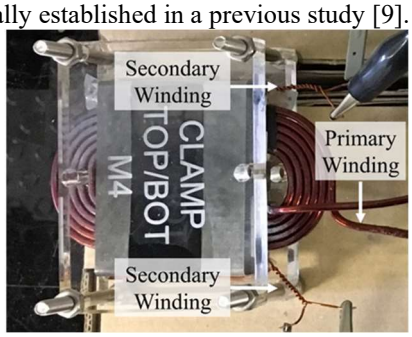


Fig. 11. Tested inductor with CoFe EE cores

An inverter-load configuration with passive RLC load as Fig. 6(b) is considered for this case study by simulation with the specifications listed in Table I, which will be implemented in a real test rig in the next section.

Table I. Specifications of the Studied Case

Fundamental frequency f_0	100 Hz	R	1.1 Ω
Switching frequency f_{sw}	10 kHz/20 kHz	L	36 µH
DC-link voltage U_{dc}	100 V	C	135 µF
U_R amplitude	35 V	I_R amplitude	31.8 A

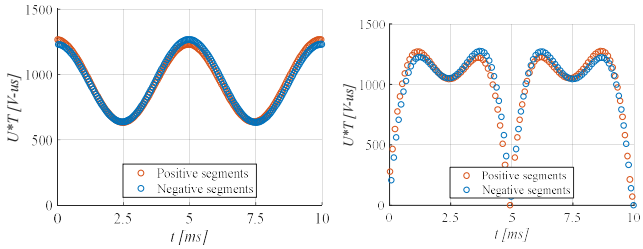
To make a comparison between the two-level and three-level topologies, two inverter setups are designed:

- Case A: 2-level converter with fsw = 20 kHz
- Case B: 3-level NPC converter with fsw = 10 kHz

The inductance of the filter inductor in the discussed configuration is designed based on the maximum peak-to-peak current ripple $\Delta I_{MAXpk\text{-}pk}$ [2]. According to [34], a three-level converter offers approximately half the $\Delta I_{MAXpk\text{-}pk}$ compared to a two-level converter when the other parameters are the same. Fig. 12 shows a comparison of the inductor voltage/current waveforms in a 2-level and a 3-level converter. It can be seen that the maximum current ripple amplitudes in Fig. 12(a) and Fig. 12(c) are equal.

Thus, if the same inductor is used, a three-level converter with $0.5f_{sw}$ can be considered equivalent to a two-level converter with f_{sw}, from the maximum current ripple point of view. Although the harmonic content of Case A and Case B are different, the filter inductors are commonly designed against the maximum current ripple rather than the harmonic content. Hence, case A and B provide a practical comparison between these two topologies with equal $\Delta I_{MAXpk\text{-}pk}$ and an identical inductor.

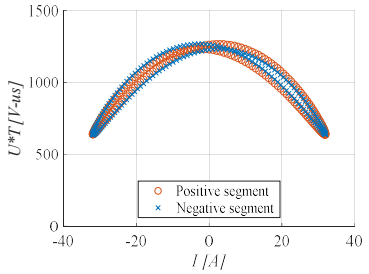
Following the developed analytical model, the operating space of the filter inductor can be generated for both cases. To utilize the user-friendly loss map, the operating space of the inductor is defined by the three variables as introduced: $|U_L T|$, $|U_L|$ and I_0. Firstly, as the fundamental factor determining the core loss and the current ripple, the voltage-time product (proportional to swing of the flux density ΔB) applied on the inductor is calculated on cycle-by-cycle basis and plotted in Fig. 13.



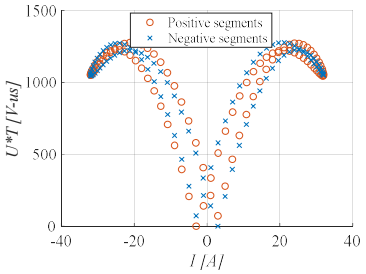
(a) case A: 2-level with f_{sw} = 20 kHz (b) case B: 3-level with f_{sw} = 10 kHz

Fig. 13. Volt-time product applied on the inductor (modulation index M = 0.7)

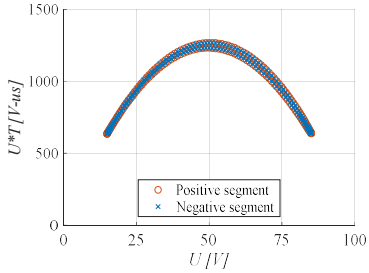
It can be seen that in both cases the maximum voltage-time product is around 1270 $V{\cdot}\mu s$, which indicates the maximum current ripple is kept the same in both cases. In the 2-level converter case, the voltage-time product swings between 640 ~ 1270 $V{\cdot}\mu s$. As indicated by expression (9), both the number of segments and the associated core loss of each segment contribute to the total core loss over a fundamental cycle. Fig. 14 illustrates the number of segments grouped by various ranges of voltage-time product. As the graph indicates, in the Case B, there are less segments operates at high voltage-time stress compared to the Case A, especially in the group 600 ~ 900 $V{\cdot}\mu s$. Due to the three-level operation, there are 26%



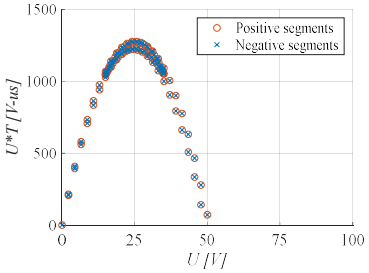
(a1) Case A: U_LT and I_0



(b1) Case B: U_LT and I_0



(a2) Case A: U_LT and U_L



(b2) Case B: U_LT and U_L

Fig. 15. Comparison of inductor operating space (modulation index M = 0.7) (a) case A: two-level with f_{sw} = 20 kHz (b) case B: three-level with f_{sw} = 10 kHz

segments in Case B operate at less than < 600 $V{\cdot}\mu s$, although the maximum U_LT is the same as the 2-level converter case at around 1270 $V{\cdot}\mu s$. Additionally, the total voltage-time products applied on the inductor for the *Case A* and *Case B* are 3.77e5 $V{\cdot}\mu s$ and 2.01e5 $V{\cdot}\mu s$ respectively. It shows that the inductor in the 3-level converter sustains approximately only half the voltage-time stress compared to the 2-level converter case.

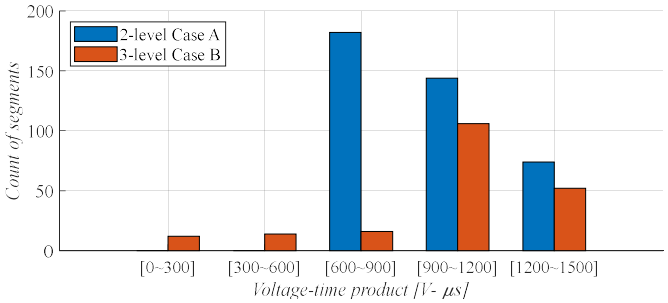
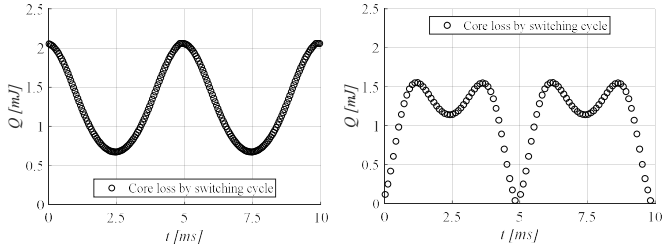


Fig. 14. Volt-time product applied on the inductor (modulation index M = 0.7)

The operating spaces of the inductor concerning the three variables (U_LT, U_L and I_0) are plotted in Fig. 15 for both cases. Fig. 15(a1) and Fig. 15(b1) show the operating space concerning the DC-bias current (proportional to H_0) and the voltage-time product. For the two-level converter, the largest flux swing of segments occurs at a low DC-bias current (i.e. I_0 ≈ 0 A). For the three-level converter, the largest flux swing of segments occurs at relatively high load current, i.e. I_0 ≈ 22 A. Due to the complex correlation between the core loss and the DC-bias (pre-magnetization) [9], [35], [36], it is difficult to draw a conclusion on judging which case of operation is better.

Fig. 15 (a2) and Fig. 15 (b2) show the operating space concerning the voltage amplitude (proportional to dB/dt) and the voltage-time product (proportional to ΔB). For the two-level converter, the U_L of segments spread evenly between 15 V ~ 85 V, with the largest U_LT occurring at U_L = 50 V. For the three-level converter, the U_L of segments concentrate at around 15 V ~ 35 V, with the largest U_LT occurring at U_L = 25 V. Therefore, it can be concluded that the three-level converter also operates the inductor at an overall lower level of U_L (dB/dt) compared to the two-level converter. Note that the core loss is positively correlated to the U_L (proportional to dB/dt or frequency f) in most cases according to the measurements in previous studies [8], [9].

Next, the calculated instantaneous core loss is plotted by switching cycles in Fig. 16 over the period of a fundamental cycle. It can be seen that the shape of the instantaneous core loss is similar to Fig. 13, because the voltage-time product is the main factor determining the core loss in the tested inductor. It can also be seen that the shape of the instantaneous core loss in the two-level converter shows two peaks over a fundamental cycle, which is also observed in [8].



(a) case A: 2-level with f_{sw} = 20 kHz (b) case B: 3-level with f_{sw} = 10 kHz

Fig. 16. Instantaneous core loss by switching cycle (M = 0.7)

By adding up the core loss of all segments, the averaged core loss for both cases are summarized in TABLE II. The simulation generated U_L/I_L waveforms are fed through the loss map for the purpose of comparison. The results show that the simulation results agree well with the analytical model. Because the load voltage is not perfectly sinusoidal, the core losses calculated from simulation waveforms show a minor discrepancy. It can be seen that the core loss of the 3-level converter (Case B) is less than half of the 2-level converter (Case A). This is an overall result contributed by the halved number of segments, smaller U_LT product of segments and less square wave amplitude U_L in the Case B of 3-level converter.

TABLE II. COMPARISON OF CALCULATED AVERAGED CORE LOSS

	Case A 2-level, f_{SW} = 20kHz	**Case B 3-level, f_{SW} =10kHz**
Calculated from U_L/I_L waveforms drawn from ideal simulation model	26.3W	11.2 W
Calculated from analytical model	26.1 W	11.1 W

Enabled by the proposed analytical calculation, the core loss can be rapidly estimated in various operating point of the power converter through a computerized tool. For example, considering the DC-link voltage is adjustable, the modulation index M and the DC-link voltage of the converter can be adjusted in pair to achieve an equivalent output voltage at fundamental frequency. In this case, the core loss is evaluated against various modulation index in MATLAB with the results plotted in Fig. 17. The result shows that the higher modulation index/lower DC-link voltage leads to the less inductor core loss. A lower DC-link voltage results in smaller amplitudes of the current ripples and the swings of flux density. Therefore, from the core loss point of view, the converter is preferred to operate at a higher modulation index and lowwe DC-link voltage to achieve the equivalent output voltage.

To summarize, the 3-level converter with halved switching frequency offers less than half the core loss on the identical inductor compared to the 2-level converter. Additionally, it has been well established that the 3-level converter can significantly reduce the device switching loss [11], [21] due to the halved switching voltage. Therefore, the 3-level converter offers further improvement of system efficiency with both the device switching loss and the inductor core loss considered.

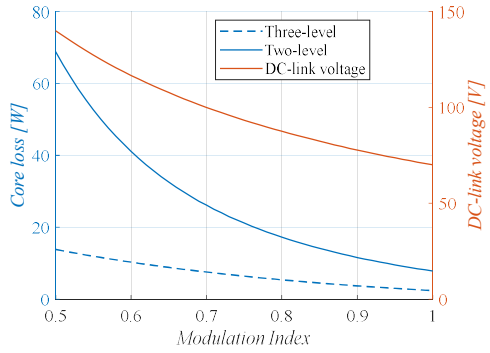


Fig. 17. Inductor core loss vs. modulation index M with and fixed output voltage , f_{sw} = 20 kHz

V. EXPERIMENTAL EVALUATION

A test rig is built for both the loss-mapping process and the inverter operation to validate the proposed calculation method. The purpose is to investigate whether the operating space and core loss of the inductor can be correctly predicted by the presented analytical model. The RLC load is configured as listed in TABLE I. A picture of the setup is shown in Fig. 18.

The inductor voltage and current are measured by high bandwidth probes and captured in a digital oscilloscope. The components and instruments in the test rig are listed in TABLE III. The power module SKiM301TMLI12E4B is based on a 3-level T-type topology as Fig. 5(b), which can operate as either a 2-level converter or a 3-level converter. This topology enables a straightforward comparison between 2-level and 3-level operations regarding the inductor core loss. The DC-link of the test rig is formed by capacitors C1 and C2 in series. The proposed approach is experimentally evaluated in this section on two example inductors to prove its validity and versatility.

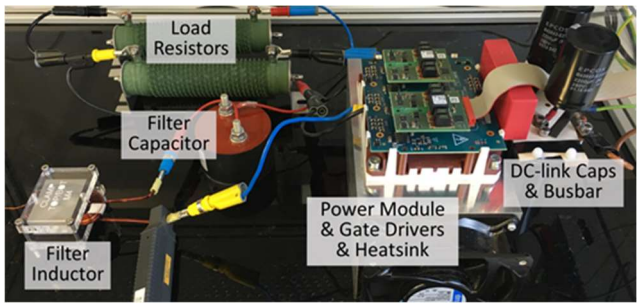


Fig. 18. Picture of the test rig

TABLE III. COMPONENTS AND INSTRUMENTS IN THE TEST RIG

DC-link capacitance	C1= C2 =2670 µF	**Power module**	SKiM301TMLI12E 4B
Digital Oscilloscope	MSO-X 3054A (500 MHz, 4 GSa/s)	**Gate Driver**	Semikron SKYPER 42 J
Voltage probe	Keysight N2862B (150 MHz)	**Current probe**	Keysight N2783B (100 MHz)

A. *Inductor 1 with gapped cobalt iron core*

Firstly, the inductor with gapped cobalt iron core shown in Fig. 11 is tested. The voltage and current waveform applied on the inductor is measured for the calculation of core loss. An example of the measured waveforms is plotted in Fig. 19. In the zoomed-in view in Fig. 19, it can be seen that the voltage applied on the filter inductor in this case is in the same manner as the waveform S in Fig. 2, which contains asymmetric rectangular excitation voltage in each switching cycle.

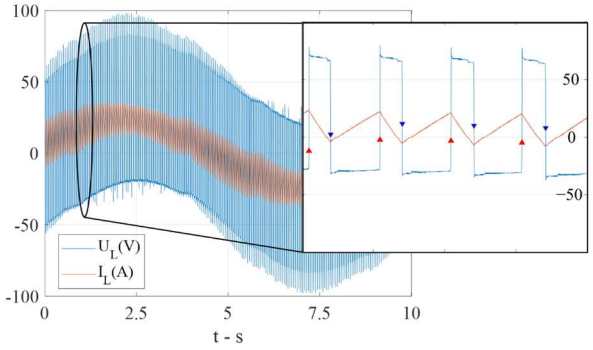
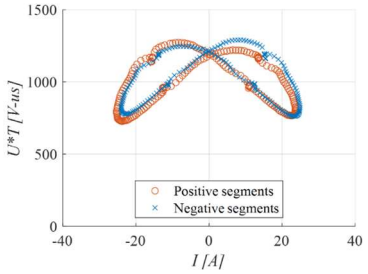
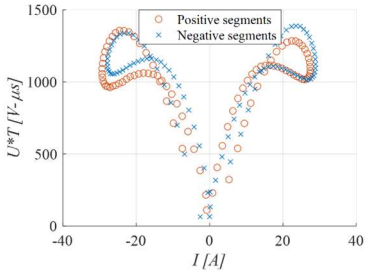


Fig. 19. Measured inductor voltage and current with segments marked in Matlab (two-level with f_{sw} = 20 kHz, M = 0.7, CoFe core)

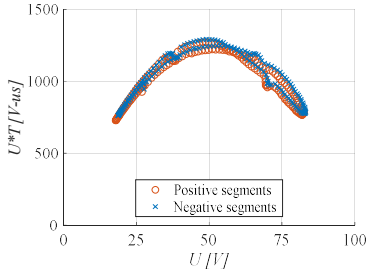
Two sets of core loss calculation process are programmed in Matlab as illustrated in Fig. 20. The first set analyses the experimentally measured voltage/current waveforms, slices the waveforms into single-pulse segments by zero-crossing detection (as illustrated in Fig. 19) and calculate the core loss as shown in Fig. 20(a). The second set is the proposed analytical model, in which the calculation starts from manual inputs as shown in Fig. 20(b). A comparison between the calculated core loss between these two sets, *Result a* and *Result b*, will verify the proposed analytical method.



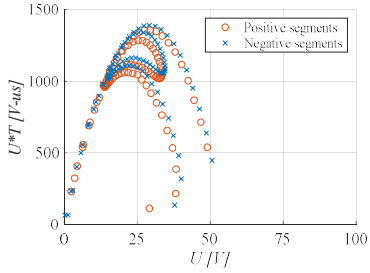
(a1) Case A: U_LT and I_0



(b1) Case B: U_LT and I_0

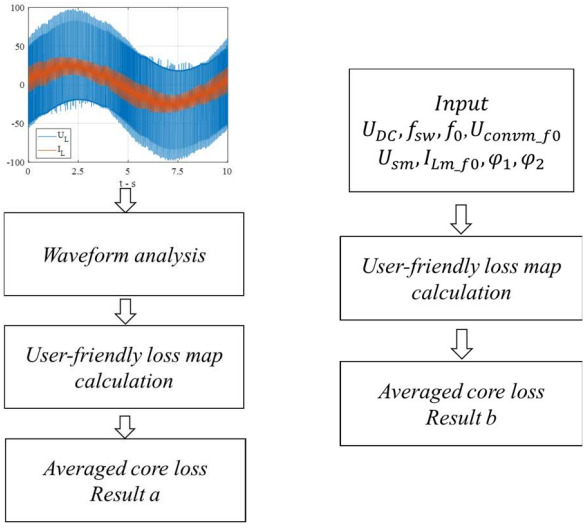


(a2) Case A: U_LT and U_L



(b2) Case B: U_LT and U_L

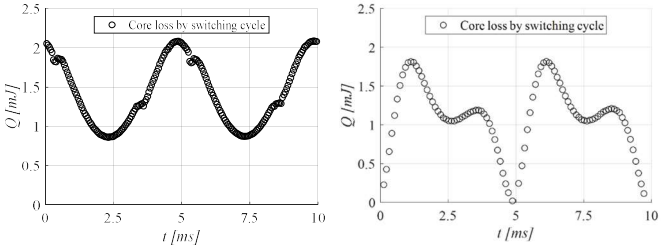
Fig. 22. Comparison of inductor operating space (modulation index M = 0.7) (a) case A: two-level with f_{sw} = 20 kHz (b) case B: three-level with f_{sw} = 10 kHz



(a) (b)

Fig. 20. The core loss computation processes (a) calculated from experimental/simulation waveforms (b) proposed analytical model

The calculated instantaneous core loss is plotted in Fig. 21 on switching cycle basis. Compared to Fig. 16, Fig. 21 shows a distorted shape compared due to the DC-link neutral point voltage oscillation in the test rig, which is not considered in the proposed analytical model. The analytical model assumes an ideal dc-link voltage supply.



(a) case A: 2-level with f_{sw} = 20 kHz (b) case B: 3-level with f_{sw} = 10 kHz

Fig. 21. Instantaneous core loss by switching cycle generated from experimentally measured waveforms, M = 0.7

The experimentally measured waveforms are analyzed with the operating space visualized in Fig. 22. The visible distortion of the operating space compared to Fig. 15 is also caused by the neutral point voltage oscillation in the test rig, which has been confirmed in the simulation models with nonideal dc-link.

A comparison of the calculated core loss through both methods are shown in TABLE IV. The *Result b* in TABLE IV is calculated with the experimentally measured amplitudes/phase angles of the voltage and currents to exclude the deviations caused by the non-ideal load parameters (e.g. manufacturing tolerance of the capacitance and parasitics on the wirings).

TABLE IV. COMPARISON OF CALCULATED AVERAGED CORE LOSS IN THE COBALT IRON INDUCTOR

	Case A 2-level f_{sw} = 20 kHz	Case B 3-level f_{sw} =10 kHz
Result a Calculated from experimentally measured U_L and I_L	28.5 W	10.6 W
Result b Calculated from analytical model	31.0 W	11.4 W

Overall, the experimental results confirm the validity of the analytical model in predicting the inductor operating space and subsequently the core loss given the converter operating point.

The discrepancy between *Result a* and *Result b* reflects the differences of loss map inputs caused by the non-ideal operation of the power converter that is not reflected in the proposed analytical model. The non-ideal factors are:

- The existence of deadtime and the trapezoidal converter output voltage (due to rise/fall time of IGBTs) instead of ideal square wave. These two factors lead to insufficiently generated pulses in the real test rig, which undermines the U_LT product of the pulse segments.
- Fluctuation of the neutral point voltage. The dc-link neutral point voltage is assumed constant in the theoretical model while it suffers a fundamental-frequency oscillation in the

test rig due to the single-phase configuration [20]

- The load-side voltage varies within one switching cycle while the analytical model assumes it to be constant

B. Inductor 2 with toroidal iron powder core

To prove the versatility of the proposed approach, the experimental validation is performed on a second setup with an iron powder toroidal inductor, which is shown in Fig. 18 mounted with the RC load on a printed circuit board.

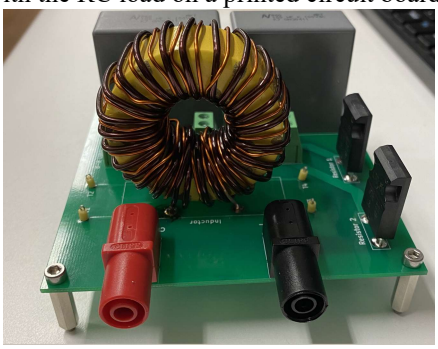


Fig. 23. Iron powder toroidal inductor mounted with RC load

This iron powder inductor has also been tested through the same loss-mapping procedure to generate its core loss data. It is then exposed in the same 2-level and 3-level PWM operation to validate the core loss model. The specifications of the iron powder inductor setup are listed in Table V.

TABLE V. SPECIFICATIONS OF THE IRON POWDER INDUCTOR CASE

Core type	T184-26 from Micrometals©
L	101 µH
R	5 Ω
C	200 µF
DC-link voltage	100 V

The core loss calculation results are shown in TABLE VI. As this inductor is designed to operate at a higher frequency, it has been tested at 50 kHz carrier frequency as well.

TABLE VI. COMPARISON OF CALCULATED AVERAGED CORE LOSS WITH TOROIRDAL IRON POWDER INDUCTOR ($M = 0.7$)

	2-level		3-level	
	20 kHz	50kHz	10 kHz	25kHz
Result a Calculated from measured U_L and I_L	15.50 W	7.29 W	1.94 W	0.86 W
Result b Calculated from analytical model	14.39 W	6.64 W	1.88 W	0.85 W

TABLE VI shows that the analytical core loss model also agrees with the experimental results in these tested cases with a discrepancy less than 10%. With the increase of switching frequency, the core loss decreases due to the smaller current ripple amplitude and volt-time product in the pulse segments. The quantified results in TABLE IV and TABLE VI shows that the core loss in a 3-level converter can be as less as only 13%-37% of an equivalent 2-level case, depending on the inductor. This is because the voltage segments applied on the inductor in a 3-level converter feature averagely smaller amplitude and smaller volt-time product as analyzed in Section IV.

VI. CONCLUSION

An analytical approach for fast calculation of the inductor operating space and subsequently the core loss in PWM converters is proposed and verified in this work as a supplement to the loss map approach. The analysis in this work contributes to the understanding and modelling of the high-frequency core loss in the PWM converters targeting higher switching frequency considering the difference between 2-level and 3-level topologies. As the pre-step of utilizing a user-friendly core loss map, the loss map inputs are generated through mathematical expressions instead of simulation models and real test rigs. The efforts of building simulation models and hardware are avoided in the proposed method for the estimation of inductor core loss, which well serves the purpose of virtual prototyping of a power converter system.

The experimental results show that the proposed approach is able to correctly predict the operating space and core loss of the inductor. As revealed by the analysis, a 3-level converter running the identical inductor generates less than half core loss compared to a 2-level converter, when the switching frequency in the 3-level converter is halved to achieve the equivalent maximum current ripple. The analytical model shows that the inductor driven by a 3-level converter sustains less voltage-time product and lower voltage amplitude in the decomposed single-pulse segments. Therefore, the converter system efficiency can benefit from the 3-level converter topology both in the reduced power device switching loss and the less inductor core loss, compared to the 2-level converter topology.

The presented analytical core loss calculation process can be easily implemented in computerized tools, such as MATLAB. It enables a fast calculation of the inductor core loss for a given PWM converter operating point. The proposed core loss calculation together with the empirical loss map form a complete “datasheet + calculation” process, which is similar to the widely accepted analytical loss modelling for power devices in PWM converters (e.g. [2], [32]). The core loss estimation is beneficial for the system-level modelling, virtual prototyping and optimization of high-switching-frequency power electronics converters in the design stage. Because the proposed approach is based on the operation principles of the converter topology, it can be applied generally regardless of the core material or the design of the inductor, as long as the loss map of the inductor/core is pre-produced.

Although the core loss data in the proposed form is currently not available from the manufacturers, it can be anticipated that the manufacturers will follow up in the future once the loss map approach is widely accepted. The user-friendly loss map only needs to be measured on one sample that represents one inductor design, which is possible to be done by the manufacturers, especially for standardized inductors. Even if the users need to conduct the loss mapping by themselves for now, it still requires only limited data points on built inductors, while infinite operating points of the PWM converter can be assessed without building the whole PWM converter hardware.

Theoretically, the presented approach can be extended to multilevel waveforms (e.g. five-level waveforms). However, the introduced Composite Waveform Hypothesis only works

well in the unit of pairs of one positive and one negative pulses. If there is a series of voltage pulses with the same polarity but different amplitudes, such as a five-level waveform, CWH is unable to accurately reflect the core loss out from tested standard rectangular waveforms due to the non-linear nature of core loss [13]. This limitation was also pointed out in [8], where an approximation approach is proposed to convert the multilevel waveform into standard segments. Further development of the theory is still subject to future investigation to fundamentally correctly model the core loss for generalized multilevel rectangular waveforms.

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